AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Original) An integrated circuit, comprising:
   a clock source that outputs a clock signal, wherein the clock signal propagates down a first path; and
   a first biasable delay driver that inputs the clock signal at a point on the first path,
   wherein the first biasable delay driver is selectively sized based on a delay of the clock signal from the clock source to the point on the first path.

2. (Original) The integrated circuit of claim 1, the first biasable delay driver comprising:
   a first element that inputs the clock signal and outputs a modulated clock signal; and
   a second element that inputs the modulated clock signal and outputs a delay biased clock signal, wherein a size of the first element is variable.

3. (Original) The integrated circuit of claim 2, wherein the second element has a fixed size.

4. (Original) The integrated circuit of claim 1, wherein the clock signal propagates down a second path, the integrated circuit further comprising:
   a second biasable delay driver that inputs the clock signal at a point on the second path, wherein the second biasable delay driver is selectively sized based on a delay of the clock signal from the clock source to the point on the second path.

5. (Original) The integrated circuit of claim 4, wherein the second path has a resistive component and a capacitive component.

6. (Original) The integrated circuit of claim 4, wherein a load on the first path and a load on the second path is unbalanced.

7. (Original) The integrated circuit of claim 4, wherein an RC delay of the first path is not equal to an RC delay of the second path.

8. (Original) The integrated circuit of claim 4, wherein a length of the first path is not equal to a length of the of the second path.

9. (Original) The integrated circuit of claim 1, wherein the first path has a resistive component and a capacitive component.

10. (Original) The integrated circuit of claim 1, wherein the clock source is a clock header.

11. (Cancelled)

12. (Original) A method for reducing clock skew, comprising:

determining a first delay of a clock signal from a clock source to a point on a first path, wherein the clock signal propagates from the clock source to the point on the first path; and

selectively sizing a first biasable delay driver depending on the first delay, wherein the first biasable delay driver inputs the clock signal at the point on the first path.

13. (Original) The method of claim 12, wherein the first path has a resistive component and a capacitive component.

14. (Original) The method of claim 12, wherein the clock source is a clock header.

15. (Original) The method of claim 12, wherein selectively sizing the first biasable delay driver comprises:

determining whether the first delay is less than a minimum delay;

if the first delay is less than a minimum delay, decreasing a size of the first biasable delay driver.

16. (Original) The method of claim 15, wherein selectively sizing the first biasable delay driver further comprises:

determining whether the first delay is greater than a maximum delay;

if the first delay is greater than a maximum delay, increasing the size of the first biasable delay driver.

17. (Original) The method of claim 16, further comprising determining a second delay of a clock signal from the clock source to a point on a second path, wherein the clock signal propagates from the clock source to the point on the second path, wherein selectively sizing the first biasable delay driver further comprises:

defining the minimum delay, wherein defining the minimum delay comprises:

defining a longest delay, wherein the longest delay is the greater of the first delay and the second delay;

defining a shortest delay, wherein the shortest delay is the smaller of the first delay and the second delay;

determining whether the longest delay minus the shortest delay is greater than a gate delay;

if the longest delay minus the shortest delay is not greater than the gate delay, setting the minimum delay to be equal to a value between the shortest delay and the longest delay depending on a range of available sizes of the first biasable delay driver,

defining the maximum delay, wherein the maximum delay is equal to the minimum delay plus an increment of the first biasable delay driver.

18. (Original) The method of claim 16, further comprising determining a second delay of a clock signal from the clock source to a point on a second path, wherein the clock signal propagates from the clock source to the point on the second path, wherein selectively sizing the first biasable delay driver further comprises:

defining the minimum delay, wherein defining the minimum delay comprises:

defining a longest delay, wherein the longest delay is the greater of the first delay and the second delay;

defining a shortest delay, wherein the shortest delay is the smaller of the first delay and the second delay;

determining whether the longest delay minus the shortest delay is greater than a gate delay;

if the longest delay minus the shortest delay is greater than the gate delay, setting the minimum delay to be equal to the longest delay minus the gate delay; and

if the longest delay minus the shortest delay is not greater than the gate delay, setting the minimum delay to be equal to the shortest delay,

defining the maximum delay, wherein the maximum delay is equal to the minimum delay plus an increment of the first biasable delay driver.

19. (Original) The method of claim 18, further comprising:

selectively sizing a second biasable delay driver depending on the second delay, wherein the second biasable delay driver inputs the clock signal at the point on the second path.

20. (Original) The method of claim 18, wherein the second path has a resistive component and a capacitive component.

21. (Original) The method of claim 18, wherein a load on the first path and a load on the second path is unbalanced.

22. (Original) The method of claim 18, wherein an RC delay of the first path is not equal to an RC delay of the second path.

23. (Currently Amended) The method of claim 18, wherein a length of the first path is not equal to a length ~~of the~~ of the second path.

24. (Original) A computer system, comprising:

a processor;

a memory; and

instructions, residing in the memory and executable by the processor, for:

determining a first delay of a clock signal from a clock source to a point on a first path, wherein the clock signal propagates from the clock source to the point on the first path; and

selectively sizing a first biasable delay driver depending on the first delay, wherein the first biasable delay driver inputs the clock signal at the point on the first path.

25. (Original) The computer system of claim 24, wherein the first path has a resistive component and a capacitive component.

26. (Original) The computer system of claim 24, wherein the clock source is a clock header.

27. (Original) The computer system of claim 24, wherein the instructions for selectively sizing the first biasable delay driver comprise instructions for:

determining whether the first delay is less than a minimum delay;

if the first delay is less than a minimum delay, decreasing a size of the first biasable delay driver.

28. (Original) The computer system of claim 27, wherein the instructions for selectively sizing the first biasable delay driver further comprise instructions for:

determining whether the first delay is greater than a maximum delay;

if the first delay is greater than a maximum delay, increasing the size of the first biasable delay driver.

29. (Original) The computer system of claim 28, further comprising instructions for determining a second delay of a clock signal from the clock source to a point on a second path, wherein the clock signal propagates from the clock source to the point on the second path, wherein the instructions for selectively sizing the first biasable delay driver further comprise instructions for:

defining the minimum delay, wherein defining the minimum delay comprises:

defining a longest delay, wherein the longest delay is the greater of the first delay and the second delay;

defining a shortest delay, wherein the shortest delay is the smaller of the first delay and the second delay;

determining whether the longest delay minus the shortest delay is greater than a gate delay;

if the longest delay minus the shortest delay is not greater than the gate delay, setting the minimum delay to be equal to a value between the shortest delay and the longest delay depending on a range of available sizes of the first biasable delay driver,

defining the maximum delay, wherein the maximum delay is equal to the minimum delay plus an increment of the first biasable delay driver.

30. (Original) The computer system of claim 28, further comprising instructions for determining a second delay of a clock signal from the clock source to a point on a second path, wherein the clock signal propagates from the clock source to the point on the second path, wherein

the instructions for selectively sizing the first biasable delay driver further comprise instructions for:

defining the minimum delay, wherein defining the minimum delay comprises:

defining a longest delay, wherein the longest delay is the greater of the first delay and the second delay;

defining a shortest delay, wherein the shortest delay is the smaller of the first delay and the second delay;

determining whether the longest delay minus the shortest delay is greater than a gate delay;

if the longest delay minus the shortest delay is greater than the gate delay, setting the minimum delay to be equal to the longest delay minus the gate delay; and

if the longest delay minus the shortest delay is not greater than the gate delay, setting the minimum delay to be equal to the shortest delay,

defining the maximum delay, wherein the maximum delay is equal to the minimum delay plus an increment of the first biasable delay driver.

31. (Original) The computer system of claim 30, further comprising instructions for:

selectively sizing a second biasable delay driver depending on the second delay, wherein the second biasable delay driver inputs the clock signal at the point on the second path.

32. (Original) The computer system of claim 30, wherein the second path has a resistive component and a capacitive component.

33. (Original) The computer system of claim 30, wherein a load on the first path and a load on the second path is unbalanced.

34. (Original) The computer system of claim 30, wherein an RC delay of the first path is not equal to an RC delay of the second path.

35. (Currently Amended) The computer system of claim 30, wherein a length of the first path is not equal to a length of the ~~of the~~ second path.

36. (Original) A computer-readable medium having recorded therein instructions executable by processing, the instructions for:

determining a first delay of a clock signal from a clock source to a point on a first path, wherein the clock signal propagates from the clock source to the point on the first path; and

selectively sizing a first biasable delay driver depending on the first delay, wherein the first biasable delay driver inputs the clock signal at the point on the first path.

37. (Original) The computer-readable medium of claim 36, wherein the first path has a resistive component and a capacitive component.

38. (Original) The computer-readable medium of claim 36, wherein the clock source is a clock header.

39. (Original) The computer-readable medium of claim 36, wherein the instructions for selectively sizing the first biasable delay driver comprise instructions for:

determining whether the first delay is less than a minimum delay;

if the first delay is less than a minimum delay, decreasing a size of the first biasable delay driver.

40. (Original) The computer-readable medium of claim 39, wherein the instructions for selectively sizing the first biasable delay driver further comprise instructions for:

determining whether the first delay is greater than a maximum delay;

if the first delay is greater than a maximum delay, increasing the size of the first biasable delay driver.

41. (Original) The computer-readable medium of claim 40, further comprising instructions for determining a second delay of a clock signal from the clock source to a point on a second path, wherein the clock signal propagates from the clock source to the point on the second path, wherein the instructions for selectively sizing the first biasable delay driver further comprise instructions for:

defining the minimum delay, wherein defining the minimum delay comprises:

defining a longest delay, wherein the longest delay is the greater of the first delay and the second delay;

defining a shortest delay, wherein the shortest delay is the smaller of the first delay and the second delay;

determining whether the longest delay minus the shortest delay is greater than a gate delay;

if the longest delay minus the shortest delay is not greater than the gate delay, setting the minimum delay to be equal to a value between the shortest delay and the longest delay depending on a range of available sizes of the first biasable delay driver,

defining the maximum delay, wherein the maximum delay is equal to the minimum delay plus an increment of the first biasable delay driver.

42. (Original) The computer-readable medium of claim 40, further comprising instructions for determining a second delay of a clock signal from the clock source to a point on a second path, wherein the clock signal propagates from the clock source to the point on the second path, wherein the instructions for selectively sizing the first biasable delay driver further comprise instructions for:

defining the minimum delay, wherein defining the minimum delay comprises:

defining a longest delay, wherein the longest delay is the greater of the first delay and the second delay;

defining a shortest delay, wherein the shortest delay is the smaller of the first delay and the second delay;

determining whether the longest delay minus the shortest delay is greater than a gate delay;

if the longest delay minus the shortest delay is greater than the gate delay, setting the minimum delay to be equal to the longest delay minus the gate delay; and

if the longest delay minus the shortest delay is not greater than the gate delay, setting the minimum delay to be equal to the shortest delay,

defining the maximum delay, wherein the maximum delay is equal to the minimum delay plus an increment of the first bias able delay driver.

43. (Original) The computer-readable medium of claim 42, further comprising instructions for:

selectively sizing a second biasable delay driver depending on the second delay, wherein the second biasable delay driver inputs the clock signal at the point on the second path.

44. (Original) The computer-readable medium of claim 42, wherein the second path has a resistive component and a capacitive component.

45. (Original) The computer-readable medium of claim 42, wherein a load on the first path and a load on the second path is unbalanced.

46. (Original) The computer-readable medium of claim 42, wherein an RC delay of the first path is not equal to an RC delay of the second path.

47. (Currently Amended) The computer-readable medium of claim 42, wherein a length of the first path is not equal to a length ~~of the~~ of the second path.